CLAIMS:

1. A method for fabricating a sensor array having a plurality of pixels each including a sensor element coupled to a sensor input (24) of an electronic processing circuit, the method comprising:

integrating the electronic processing circuits (25, 26) on a wafer (20) so as to form an integrated circuit having at least one array of electronic processing circuits each electronic processing circuit having a respective sensor input (24) and the integrated circuit having a plurality of terminal nodes, the sensor inputs and the terminal nodes being disposed toward a first surface of the wafer, and

in respect of either each pixel or each terminal node, providing an electrically conductive via (31) through the wafer (20) extending from either the respective sensor input (24) or from the respective terminal node to a second surface (28) of the wafer opposite the first surface;

thus allowing each electrically conductive via (31) exposed at the second surface of the wafer to serve for connection thereto of either a sensor element or a terminal connection that is electrically connected through the electrically conductive via (31) to the respective sensor input or terminal node.

2. The method according to Claim 1, wherein the electrically conductive vias serve to connect respective sensor elements to respective sensor inputs and there is further included:

growing the sensor elements on the second surface of the integrated circuit, each in registration with a corresponding one of the electrically conductive vias.

3. The method according to Claim 1, wherein the electrically conductive vias serve to connect respective terminal pads to respective terminal nodes and there is further included:

growing the sensor elements on the first surface of the integrated circuit, with the terminal nodes in registration with respective electrically conductive vias.

4. The method according to any one of Claims 1 to 3, wherein the integrated circuit includes multiple arrays of pixels and there is further included:

dividing the integrated circuit into discrete sensor arrays.

5. The method according to any one of Claims 1 to 4, further including:

assembling multiple sensor arrays edge to edge so as to form a composite sensor array having an extended surface area.

6. The method according to any one of Claims 1 to 5, further including:

thinning down the wafer (29) from a reverse side (28) thereof so as to remove the bulk of the wafer.

7. The method according to any one of Claims 1 to 5, wherein the wafer (20) is pre-thinned prior to providing the electrically conductive vias (31) through the wafer (20).

8. The method according to any one of Claims 1 to 7, wherein providing electrically conductive vias (31) through the wafer (20) includes:

coating the first surface of the wafer (20) with photomask (30) for protecting an area surrounding the sensor inputs or the terminal nodes (24), whilst leaving the sensor inputs or the terminal nodes (24) exposed, and

implanting the wafer with a material to which the photomask (30) is impervious, so that said material penetrates only the sensor inputs (24) or the terminal nodes and creates a local increase in the conductivity of the wafer from the sensor inputs (24) or the terminal nodes through the wafer (20) to the second surface thereof, thus forming a matrix of conductive vias (31), each of which connects a respective sensor input (24) or terminal node to the second surface of the wafer (20).

9. The method according to Claim 8, further including:

producing a complementary photomask that covers said area of the wafer on the second surface thereof and is in precise registration with the photomask (30) that is disposed on the first surface thereof.

10. The method according to Claim 8 or 9, wherein the wafer is based on silicon and said material is a p-type impurity.

11. The method according to any one of Claims 1 to 7, wherein providing electrically conductive vias (31) through the wafer (20) includes:

providing a photomask on the second surface only of the wafer so as to expose the wafer in direct registration with the sensor inputs or the terminal nodes on the first surface of the wafer,

etching holes through the wafer from the second surface to the sensor inputs or to the terminal nodes (24), whilst not etching all the way through the wafer so as to form bores, and

filling the bores with conductive material.

12. The method according to any one of Claims 1 to 7, wherein providing electrically conductive vias (31) through the wafer (20) includes:

partially etching holes through the wafer from the second surface so as to form partial bores,

implanting the wafer from the first surface thereof with a material to which the photomask (30) is impervious, so that said material penetrates only the sensor input (24) or the terminal node and renders the wafer conductive directly abutting each sensor input or terminal node, and

filling the partial bores with conductive material which abuts the wafer and completes the ohmic contact to the second surface of the wafer.

13. The method according to any one of Claims 1 to 7, wherein the electrically conductive vias (31) are formed in the wafer (20) prior to formation of the processing circuits by:

coating the first surface of the wafer (20) with photomask (30) for protecting an area surrounding an intended location of each sensor input or terminal node (24), whilst leaving said area exposed, and

implanting the wafer with a material to which the photomask (30) is impervious, so that said material penetrates only said area and creates a local increase in the conductivity of the wafer from the intended location of each sensor input or terminal node through the wafer (20) to the second surface thereof, thus forming a matrix of conductive vias (31) through the wafer (20).

14. The method according to any one of Claims 1 to 7, wherein the electrically conductive vias (31) are formed in the wafer (20) prior to formation of the processing circuits by:

coating the first surface of the wafer (20) with photomask (30) for protecting an area surrounding an intended location of each sensor input or terminal node (24), whilst leaving said area exposed, and

implanting the wafer with a material to which the photomask (30) is impervious, so that said material penetrates only said area and creates a local increase in the conductivity of the wafer from the intended location of each sensor input (24) or terminal node through the wafer (20) to the second surface thereof, thus forming a matrix of conductive vias (31) through the wafer (20).

15. The method according to any one of Claims 1 to 7, wherein the electrically conductive vias (31) are formed in the wafer (20) prior to formation of the processing circuits by:

providing a photomask on the second surface only of the wafer so as to expose the wafer in direct registration with respective locations on the first surface of the wafer of intended sensor inputs or terminal nodes,

etching holes through the wafer from the second surface to said locations (24), whilst not etching all the way through the wafer so as to form bores, and

filling the bores with conductive material.

16. The method according to any one of Claims 1 to 7, wherein the electrically conductive vias (31) are formed in the wafer (20) prior to formation of the processing electronics by:

partially etching holes through the wafer from the second surface so as to form partial bores,

implanting the wafer from the first surface thereof with a material to which the photomask (30) is impervious, so that said material penetrates only the intended sensor input (24) or the intended terminal node and renders the wafer conductive directly abutting each intended sensor input or terminal node, and

filling the partial bores with conductive material which abuts the wafer and completes the ohmic contact to the second surface of the wafer.

17. The method according to any one of Claims 1 to 16, wherein the electrically conductive vias (31) serve to connect respective sensor elements to respective sensor inputs and there is further included:

growing amorphous or polycrystalline sensor material on the second surface of the wafer so as to form an array of diodes each having an anode which is in ohmic contact with a respective one of the conductive vias (31) and such that the first surface of the sensor material forms a common cathode.

18. The method according to any one of Claims 1 to 12, wherein the electrically conductive vias (31) serve to connect respective terminal connections to respective terminal nodes and there is further included:

growing amorphous or polycrystalline sensor material on the first surface of the wafer so as to form an array of diodes, each having an anode which is in ohmic contact with a respective one of the sensor inputs and such that the second surface of the sensor material forms a common cathode, and

forming on the second surface of the wafer a plurality of metallized terminal pads each in ohmic contact with a respective one of the electrically conductive vias.

19. The method according to any one of Claims 13 to 18, wherein the sensor material and the terminal connections are formed on the wafer (20) prior to formation of the processing circuits (25, 26).

20. The method according to any one of Claims 1 to 19, wherein the integrated circuit includes multiple arrays of electronic processing circuits (25, 26) separated by scribe lines and there is further included:

scribing along the scribe lines so as to produce individual sensor chips (40).

21. The method according to any one of Claims 1 to 20, further including:

connecting terminal pads (43) metallized on an outer surface of the wafer via bump-bonds (45) to a ceramic board (46) that feeds bump-connections (47) through to surface mounted pins or bores, and

encapsulating so as to form a module (48).

22. The method according to Claim 21, further including:

mounting several of said modules (48) edge to edge so as to form a two-dimensional sensor (50) of larger surface area than a single module.

23. A sensor array or module manufactured according to any one of Claims 1 to 22.

24. A sensor array having a plurality of pixels each including a sensor element coupled to a sensor input (24) of an electronic processing circuit, the sensor array comprising:

a wafer having integrated therein the electronic processing circuits (25, 26) so as to form an integrated circuit having at least one array of electronic processing circuits (25, 26) each electronic processing circuit having a respective sensor input (24) and the integrated circuit having a plurality of terminal nodes, the sensor inputs and the terminal nodes being disposed toward a first surface of the wafer, and

in respect of either each pixel or each terminal node, an electrically conductive via (31) through the wafer (20) extending from either the respective sensor input (24) or from the respective terminal node to a second surface (28) of the wafer opposite the first surface and serving for electrical connection of either a respective sensor element or a respective terminal connection through the respective electrically conductive via (31) to the respective sensor input or terminal node.

REPLACED BY ART 34 AMDT

AMENDED CLAIMS

[received by the International Bureau on 2nd September 2003 (02.09.03) ; original claims 23 and 24 replaced by original claims 24 and 25 ; new claims 23 and 26 added ; remaining claims unchanged]

22. The method according to Claim 21, further including:

mounting several of said modules (48) edge to edge so as to form a two-dimensional sensor (50) of larger surface area than a single module.

23. The method according to any one of the preceding claims, when used to fabricate a sensor array for a high energy photon imaging detector.

24. A sensor array or module manufactured according to any one of Claims 1 to 23.

25. A sensor array having a plurality of pixels each including a sensor element coupled to a sensor input (24) of an electronic processing circuit, the sensor array comprising:

a wafer having integrated therein the electronic processing circuits (25, 26) so as to form an integrated circuit having at least one array of electronic processing circuits (25, 26) each electronic processing circuit having a respective sensor input (24) and the integrated circuit having a plurality of terminal nodes, the sensor inputs and the terminal nodes being disposed toward a first surface of the wafer, and

in respect of either each pixel or each terminal node, an electrically conductive via (31) through the wafer (20) extending from either the respective sensor input (24) or from the respective terminal node to a second surface (28) of the wafer opposite the first surface and serving for electrical connection of either a respective sensor element or a respective terminal connection through the respective electrically conductive via (31) to the respective sensor input or terminal node.

26. The sensor array according to Claim 25, being configured for use in a high energy photon imaging detector.

REPLACED BY
ART 34 AMDT

Referring to Fig. 7 there is shown a subsequent stage in the manufacturing process where desired amorphous or polycrystalline sensor material such as mercury iodide is grown on the top side of the wafer so as to form an array of diodes, each having an anode which is in ohmic contact with a respect one of the conductive vias 31 (shown in Fig. 6) and such that the opposite, exposed, surface of the sensor material forms a common cathode towards which incident photons are directed. Thus, Fig. 7 shows pictorially a composite wafer 35 having a lower silicon wafer 36 as described above, on top of which is grown an amorphous or polycrystalline sensor material 37 so as to form a matrix of sensor elements having a common cathode constituted by the upper surface of the device and a respective anode (not shown) that is effectively sandwiched between the upper sensor layer 37 and the lower silicon wafer 36 and is connected via a corresponding one of the vias formed in the silicon wafer 36.

As shown in Fig. 8, the wafer 35 is now scribed along the scribe lines so as to produce individual sensor chips 40, which in the specific example shown in the figure comprises 5 x 3 pixel elements in a two-layer structure having an upper layer 41 formed of a silicon wafer and having integrated therewith pixel electronics reference 23 in Fig. 4 and having a lower layer 42 on which the sensor elements themselves are deposited. Toward the upper layer 41 are also formed terminal nodes to allow for the external connection to the pixel electronics of power, I/O and control connections. This is typically done by means of terminal pads 43, which are metallized on the outer surface of the silicon wafer in known manner and formed already in an earlier stage of the fabrication corresponding to the silicon wafer 20 shown in Fig. 2. In use, access to an individual pixel in the sensor array is achieved by addressing the required pixel and the location of an active pixel in the sensor array is likewise determined by decoding its address. In a sensor array having, for example, 1024 pixels the required address bus has 10 lines and in general the required address bus for a pixel array having N pixels has $\log_2 N$ lines. Thus far fewer terminal nodes are required than sensor inputs.

each of which is fixed on a respective one of the signal takeout electrodes. A passivation film covers each signal takeout electrode where not in contact with its bump, and covering the clearances between the signal takeout electrodes. A base plate is provided with a plurality of contact pads corresponding to and in contact with the bumps.

SUMMARY OF THE INVENTION

It is thus an object of the invention to provide an improved low-cost pixel sensor, which is amenable to closer packing, obviates the above-mentioned drawbacks that are contingent on the use of bump-bonding and the provision of I/O control-pads and allows multiple sensor modules to be juxtaposed so as to form a larger area sensor without requiring any further manufacturing process after assembly.

These objects are realized in accordance with the invention by a method for fabricating a sensor array having a plurality of pixels each including a sensor element coupled to a sensor input of an electronic processing circuit, the method comprising:

integrating the electronic processing circuits on a wafer so as to form an integrated circuit having at least one array of electronic processing circuits each electronic processing circuit having a respective sensor input and the integrated circuit having a plurality of terminal nodes, the sensor inputs and the terminal nodes being disposed toward a first surface of the wafer, and

in respect of either each pixel or each terminal node, providing an electrically conductive via through the wafer extending from either the respective sensor input or from the respective terminal node to a second surface of the wafer opposite the first surface;

thus allowing each electrically conductive via exposed at the second surface of the wafer to serve for connection thereto of either a sensor element or a terminal connection that is electrically connected through the electrically conductive via to the respective sensor input or terminal node.